

Fully Integrated 5.35-GHz CMOS VCOs and Prescalers

Chih-Ming Hung, *Member, IEEE*, Brian A. Floyd, *Student Member, IEEE*, Namkyu Park, and Kenneth K. O, *Member, IEEE*

Abstract—Two 5.35-GHz monolithic voltage-controlled oscillators (VCOs) and two prescalers have been fabricated in a digital 0.25- μm CMOS process. One VCO uses p⁺/n-well diodes, while the other uses MOS varactors. Q of 57 at 5.5 GHz and 0-V bias (low- Q condition) for a p⁺/n-well varactor has been achieved. For an MOS varactor, it is possible to achieve a quality factor of 140 at 5.5 GHz. The tuning ranges of the VCOs are >310 MHz, and their phase noise is <−116.5 dBc/Hz at a 1-MHz offset while consuming ~7 mW power at $V_{DD} = 1.5$ V. The low phase noise is achieved by using only PMOS transistors in the VCO core and by optimizing the resonator layout. The prescalers utilize a variation of the source-coupled logic. The power consumption is 4.1 mW at 1.5-V V_{DD} and 5.4 GHz. By widening the transistors in the first three divide-by-two stages, the maximum operating frequency is increased to 9.96 GHz at $V_{DD} = 2.5$ V.

Index Terms—CMOS, injection-locking, MOS capacitor, prescaler, self-oscillation, varactor, voltage-controlled oscillator.

I. INTRODUCTION

FIVE-GIGAHERTZ wireless applications such as high-performance radio local-area network are gaining momentum. The requirements of a frequency synthesizer for such applications are low power, low cost, and low phase noise. Within the synthesizer, the voltage-controlled oscillator (VCO) and prescaler are the two most challenging subcircuits. For the VCO, the varactor Q degrades as the operating frequency is increased, while scaled MOS transistors required for 5-GHz operation have increased $1/f$ noise and a reduced supply, which decreases the voltage swing. All of these could make it difficult to achieve low phase noise at 5 GHz. In this paper, two 5.35-GHz VCOs having low-phase-noise performance are presented. One uses p⁺/n-well diode varactors (VCO1), while the other uses MOS varactors (VCO2). The advantages and disadvantages of using these two types of varactors will be discussed. Two frequency dividers capable of achieving low power consumption and high operating frequency are also presented. The circuits have been implemented in a 0.25- μm CMOS process with five metal layers on p[−] substrates. To minimize $1/f$ and white noise, PMOS transistors are exclusively

used in the VCO core. The prescalers utilize a variation of the source-coupled logic (SCL) [1] to reduce the switching noise and power consumption.

II. VOLTAGE-CONTROLLED OSCILLATORS

A. Transistor Noise

In the 0.25- μm CMOS process, both NMOS and PMOS transistors are surface channel devices. A concern is that PMOS transistors may have the same poor $1/f$ noise performance as NMOS transistors. However, measurements show that the PMOS $1/f$ noise is ~8–10 times smaller at 100 kHz for the same transistor dimension and gate over drive ($V_{GT} = V_{GS} - V_T$) when the V_{GT} is smaller than ~0.3 V. Considering that a PMOS transistor has lower mobility, PMOS $1/f$ noise should be even lower at a given current and transconductance (gm) due to a larger gate area [2]. In addition, the hot carrier effect in a PMOS transistor is typically smaller [3]. This is especially important in a deep submicrometer CMOS process where hot electron noise (white noise) is significant. Thus, utilization of only PMOS transistors in the VCO core should reduce the phase noise in the $1/f^3$ region (resulting from $1/f$ noise) as well as the phase noise in the $1/f^2$ region, which is mainly from the device white noise [4].

B. Circuit Design

Both VCOs use the same circuit topology shown in Fig. 1 [5]. Cross-coupled transistors M_1 and M_2 form a positive feedback loop to provide negative resistances to cancel the loss in the LC tanks. M_4 , M_5 , L_3 , and L_4 form buffers for driving 50 Ω (spectrum analyzer). By using a PMOS transistor (M_3) at the bottom, the phase noise contributed from the low frequency noise of a bias circuitry can be reduced [5]. However, the bias condition of the VCO core will have a strong dependence on V_{DD} if the gate of M_3 ($V_{g,m3}$) is controlled by a voltage source. That is, the tail current and dc voltages at drain nodes of M_1 and M_2 would change when the supply voltage varies. The AM and FM noise would therefore be significant, and the phase noise performance would be degraded. Hence, a bias circuitry is needed to reduce the variation of the bias condition.

The bias circuitry is also shown in Fig. 1, consisting of a current mirror (M_{N1} and M_{N2}) and two diode-connected PMOS transistors (M_6 and M_7). The W/L ratios of M_6 and M_7 were scaled down by ~48 times from the equivalent half-circuit of the VCO core to reduce power consumption of the bias circuit. Since M_7 replicates the bias condition of M_1 , which is diode connected at dc, the source voltages of M_3 and M_6 are the same.

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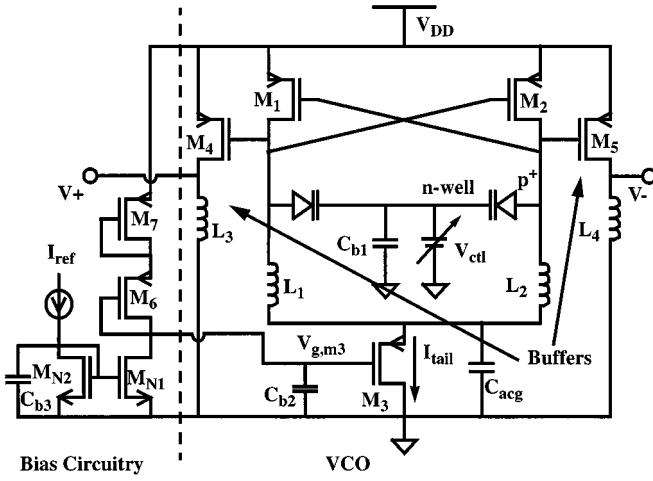


Fig. 1. A VCO circuit schematic.

The gate-to-source voltage (V_{gs}) of M_6 , which is kept constant by the current mirror at the bottom, is replicated in M_3 to keep the bias current of the VCO constant. W/L ratios for both M_{N1} and M_{N2} were chosen to be reasonably large to increase the voltage range of $V_{g,m3}$ while keeping M_{N1} in saturation. To increase the output resistance of M_{N1} , a longer channel length MOSFET was used. The channel length and width of M_{N1} and M_{N2} are 1.74 and 96 μm , respectively. The power consumption of the bias circuitry is designed to be less than 4% of that of the VCO core. The drain node of M_{N2} is bypassed to ground using a 20-pF on-chip capacitor. Measurements show that the bias circuitry has immeasurable effects on the overall phase noise performance.

The LC tanks of the VCOs are formed using an inductor with a silicided polysilicon patterned ground-shield (PGS) [6], the parasitic capacitances of M_1 and M_2 (C_{gb} , C_{gs} and C_{db}), and a p^+ /n-well diode array for VCO1 and an MOS varactor [7], [8] for VCO2. The inductance was chosen to be as large as possible (~ 1 nH) for lower power consumption while maintaining a sufficient frequency tuning range. The measured inductor characteristic is shown in Fig. 2. The quality factor using a bandwidth definition for Q (Q_{bw}) [9] is seven at 5.5 GHz. The layout and wiring of the transistors and varactors are optimized to maximize Q (Fig. 3). Since the metal connections for the gate and drain of transistors M_1 and M_2 [Fig. 3(a)] are in parallel and next to each other, the gate connection of M_1 (M_2) can be horizontally aligned to the drain connection of M_2 (M_1). This avoids a cross-connection in different metal layers, which would induce a mismatch in capacitance. The source diffusions are tied to n-substrate diffusions by silicide without using contacts to reduce the area. The measured Q versus frequency plots for the MOS varactor at -0.4 -V gate bias and the diode and total transistor parasitic capacitance at 0-V bias (low Q condition) are also shown in Fig. 2, and are 60, 57, and 25, respectively, at 5.5 GHz.

C. MOS Varactors Versus p^+ /n-well Varactors

In addition to the p^+ /n-well varactor, an MOS capacitor that has a voltage-dependent capacitance is another candidate for varactor applications [7], [8]. The MOS varactor structure has

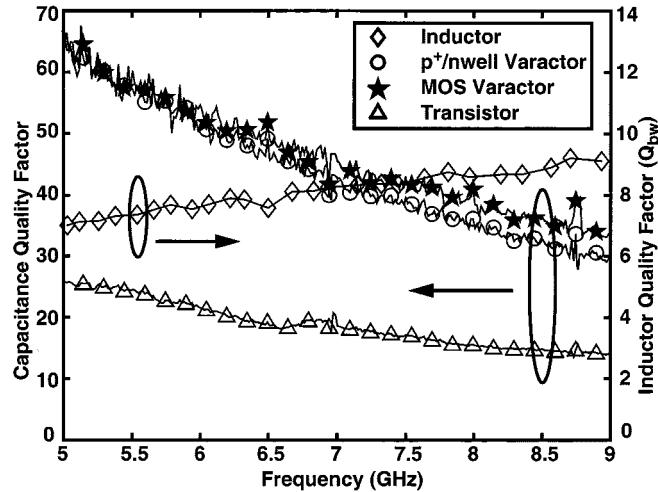


Fig. 2. Quality factors of the passive components present in the LC tank. The bias conditions of the p^+ /n-well varactor and the transistor parasitic capacitances are 0 V, while the bias voltage for the MOS varactor is -0.4 V.

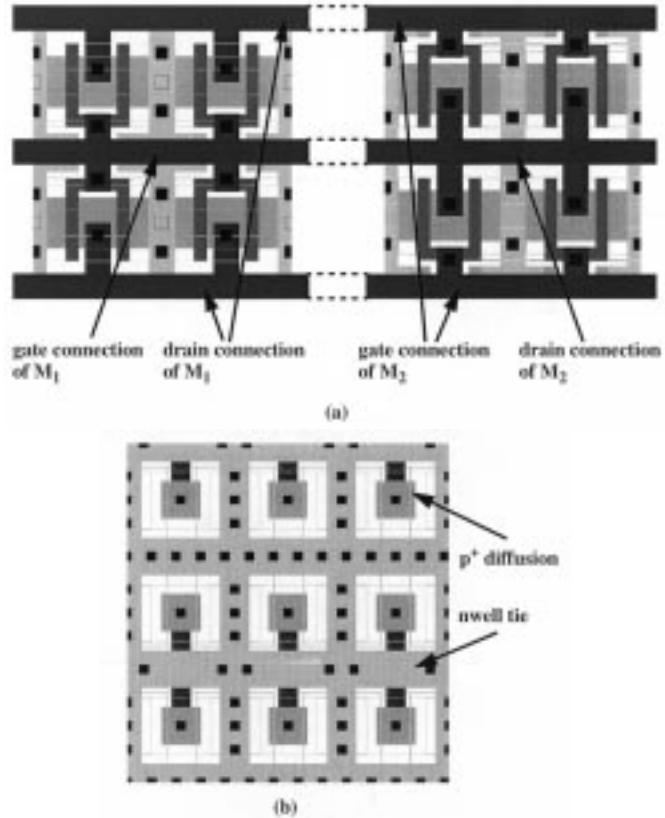


Fig. 3. (a) A partial layout of the cross-connected PMOS transistors. The source diffusions are shorted to n-well ties using the silicide to reduce the layout area. (b) A partial layout of a p^+ /well varactor.

an advantage of achieving higher quality factor. The series resistance originating from the n-well and polysilicon gate can be made smaller than the resistance from the metal interconnect [7], especially in a deep submicrometer CMOS process where gate length and width can be made very small. In addition, the number of contacts and vias for both the top and bottom plates of an MOS varactor can be increased to reduce the overall resistance contribution from these contacts and vias. The ultimate

limitation of Q for an MOS varactor in a deep submicrometer process is from the total series resistance of the metal interconnects, contacts, and vias needed for the MOS varactor layout. In the $0.25\text{-}\mu\text{m}$ CMOS process, a Q of as high as 140 for an MOS varactor at 5.5 GHz has been measured. On the other hand, the series resistance of the $p^+/\text{n-well}$ varactor mainly originates from the n-well resistance between p^+ and n^+ diffusions. Because the minimum n-well width in this structure is much larger than the minimum gate length of an MOS varactor, the maximum Q of the $p^+/\text{n-well}$ varactor is lower than that of the MOS varactor.

The voltage range needed to bias an MOS varactor from depletion to accumulation regions of operation is typically less than 2 V. Thus, an MOS varactor is naturally suitable for low voltage operation. Furthermore, because the bias voltage and thus capacitance range does not need to be limited like that for a $p^+/\text{n-well}$ varactor to avoid turning on the diode, an MOS varactor potentially has a larger tuning range. Since the voltage dependence of the MOS varactor capacitance between depletion and accumulation regions is more linear than that of a $p^+/\text{n-well}$ varactor, the frequency linearity of a VCO using MOS varactors should be better than that using $p^+/\text{n-well}$ varactors.

D. Measurement Results

An output of the VCO using $p^+/\text{n-well}$ varactors (VCO1) is connected to a spectrum analyzer through an external amplifier with a gain of 24 dB and a noise figure of 4.2 dB. With 1.5-V V_{DD} and control voltage (V_{ctl}) and 4.7-mA tail current, the measured center frequency is 5.35 GHz. The corresponding single sideband (SSB) phase noise plot is shown in Fig. 4(a). The phase noise at 100-kHz and 1-MHz offsets is -93 and -117 dBc/Hz, respectively. This VCO consumes less power and has phase noise that is more than 7 dB lower than that of the previously published 5-GHz CMOS VCOs [10], [11]. If the tail current and V_{DD} are increased to 6 mA and 2.5 V, the phase noise at the 1-MHz offset can be decreased to -119 dBc/Hz. An oscillation frequency versus V_{ctl} plot is shown in Fig. 4(b) (solid line). The tuning range is 336 MHz for V_{ctl} between 0.1 and 1.5 V. The phase noise is degraded by 3 dB at $V_{ctl} = 0.1$ V. Also shown in Fig. 4(a) is the SSB phase noise plot of the VCO using MOS varactors (VCO2). V_{DD} , V_{ctl} , and I_{tail} are 1.5 V, 0.3 V, and 4.7 mA, respectively, and the corresponding carrier frequency and phase noise are 5.23 GHz and -116.5 dBc/Hz at a 1-MHz offset, respectively. The control voltage is chosen such that the MOS varactor is at its high- Q (which is ~ 60 in this particular VCO) condition. Since the quality factor of the varactors is much higher than the inductor Q (~ 7 at 5.5 GHz), as expected, the phase noise performance of VCO2 is similar to that of the VCO1. If the oscillation frequency were increased to much higher than 5.5 GHz, the inductor Q could be significantly higher. In this situation, the tank Q can be limited by the varactor Q , and it would be beneficial to use MOS varactors with higher Q for the LC-resonators. The frequency tuning characteristic of VCO2 is also shown in Fig. 4(b) (dashed line). The tuning range is ~ 310 MHz for V_{ctl} between 0 and 1.5 V. The phase noise variation is less than 1 dB over the entire tuning range. As discussed earlier, the tuning characteristic is more linear compared

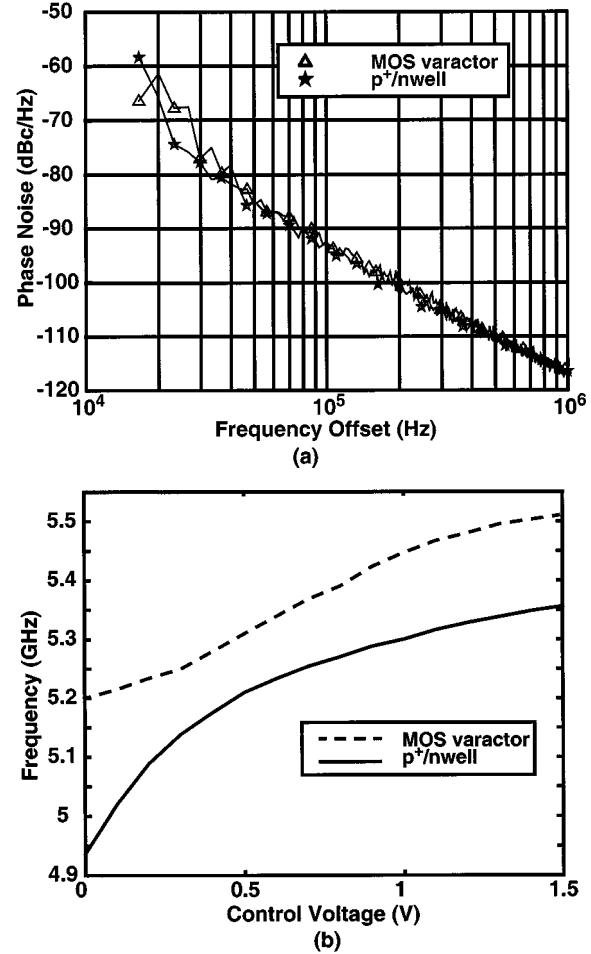


Fig. 4. (a) SSB phase noise plots for VCO1 (“*”) and VCO2 (“ Δ ”). V_{DD} and the tail current are 1.5 V and 4.7 mA, respectively. (b) The VCO tuning characteristics for VCO1 (solid line) and VCO2 (dashed line).

to that of VCO1. The performance of both VCOs is summarized in Table I.

III. PRESCALERS

A. Circuit Design

The divide-by-128 prescaler is designed using seven cascaded divide-by-two circuits, shown in Fig. 5, followed by a three-stage inverter chain for driving the $50\text{-}\Omega$ input impedance of a measurement system. To reduce the switching noise, an SCL structure is used. The voltage swing is kept as small as possible at every node except for the first stage to avoid hard switching of the clock transistors (M_1 and M_2). The first stage inputs are driven by the VCO outputs, which typically have a large amplitude for lower phase noise. The small voltage swing also helps to increase the maximum speed since the time needed to toggle the logic state is shorter. The current source between the sources of M_1 and M_2 and ground in conventional SCL design is omitted for 1.5-V operation. V_{bias} of the first two stages are grounded to increase the maximum operating frequency by operating M_7 and M_8 in the linear region, which lowers the RC time constant for Q and \bar{Q} nodes. Furthermore, when the voltage of Q is increasing (during a

TABLE I
A SUMMARY OF THE PERFORMANCE FOR THE VCOs AND PRESCALERS

Technology	0.25 μ m CMOS	
Substrate Type	p ⁺ substrate	
VCOs		
Carrier (GHz)	VCO1	VCO2
SSB Phase Noise (dBc/Hz @ offset)	-93 @ 100 kHz -117 @ 1 MHz	-93 @ 100 kHz -116.5 @ 1 MHz
Tuning Range (GHz)/Vctl (V)	5.02/0.1 - 5.356/1.5	5.2/0 - 5.51/1.5
Power Consumption	4.7 mA @ 1.5 V	
Prescaler		
Division Ratio	128	
Maximum Operating Frequency (GHz)	5.4 @ 1.5 V, 2.7 mA 8.4 @ 2.5 V, 8 mA	
Maximum Operating Frequency (GHz) with Larger Design Current	9.96 @ 2.5 V, 7.36 mA for the first divide-by-8 circuit	

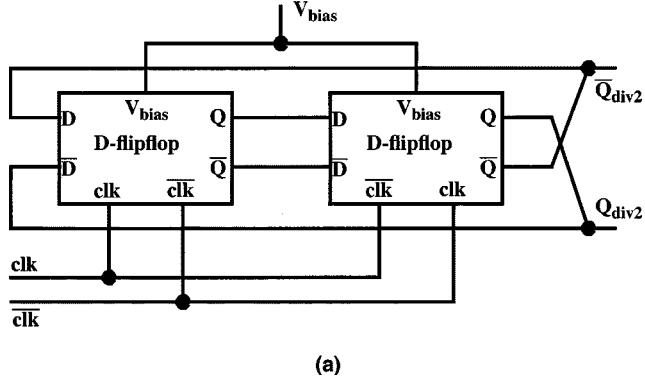


Fig. 5. (a) Block diagram of the divide-by-two circuit. (b) Circuit schematic of the D-flip-flop.

LOW-to-HIGH transition), the resistance looking up to M_8 from Q is decreased since v_{ds} and the output resistance of M_8 (in linear region) are decreased. This nonlinearity of M_8 helps to pull up Q to its logic HIGH, which in turn helps to increase the maximum operating frequency at the same power consumption. Similarly, when Q is decreasing, the nonlinearity tends to push down Q to its logic LOW. In addition to the advantage of high-speed operation, this topology has reduced

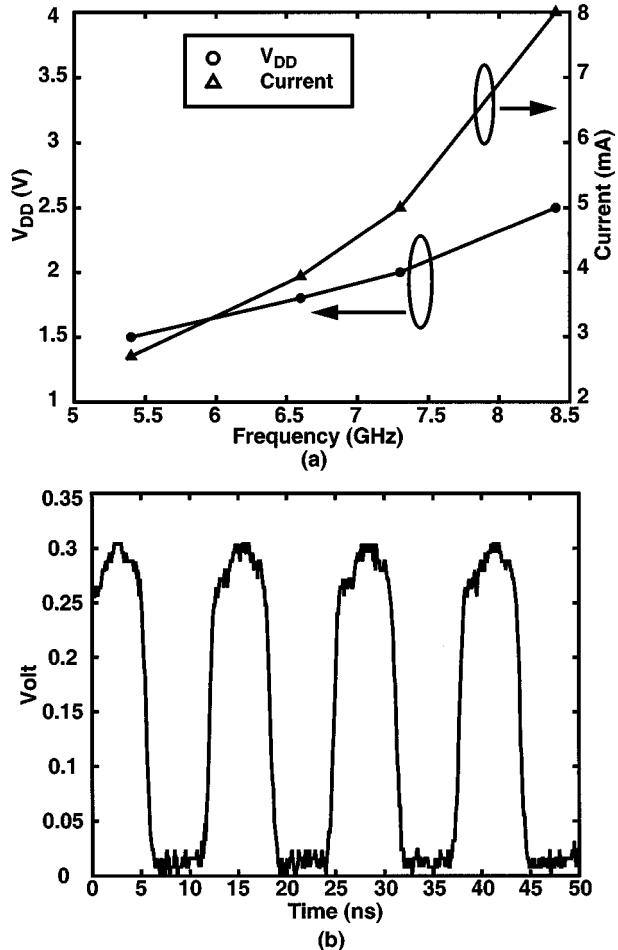


Fig. 6. (a) V_{DD} and current versus maximum operating frequency plots for the divide-by-128 prescaler. (b) An output waveform of the second prescaler (divide-by-eight) with wider M_1 , M_2 , M_7 , and M_8 at an input frequency of 9.96 GHz.

power consumption compared to the topology in [12] due to the elimination of the folded diode-connected transistors from Q and \bar{Q} to ground. The transistor sizes were chosen such that the dc level and small-signal swing at the output of each stage can directly drive the subsequent stage without fully restoring the signal level. This further reduces power consumption and lowers switching noise. To decrease the coupling of the noise from the prescaler to the integrated VCO, large-area substrate contacts are used to isolate the circuit blocks from each other.

The divide-by-two circuit may be interpreted as an injection-locked oscillator [11]. When both clock transistors (M_1 and M_2) are turned on, the divide-by-two circuit oscillates at a half of the frequency of the input signal [13]. If the input signal level is smaller than that required for injection locking to occur or the frequency of the input signal is outside of the locking range, the divide-by-two circuit self-oscillates at a frequency determined by the delay time of the flip-flop. The delay time and thus the self-oscillation frequency varies with both the bias condition and the transistor sizes. When the input frequency is away from (both above and below) twice the self-oscillation frequency, the required input power is larger. The sensitivity is maximized at an input frequency twice the self-oscillation frequency.

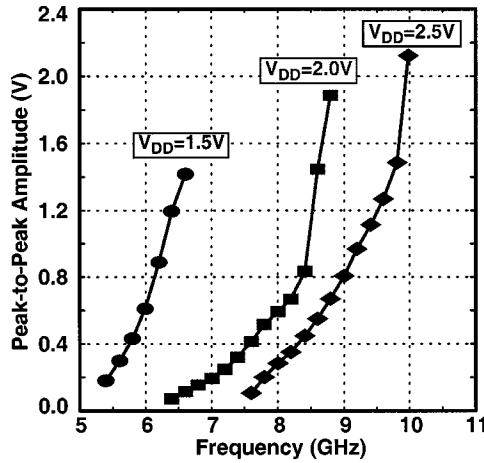


Fig. 7. Minimum peak-to-peak voltage amplitude for the input signal versus operating frequency plots at different supply voltages (V_{DD}) for the second prescaler with wider M_1 , M_2 , M_7 , and M_8 .

By increasing the sizes of M_1 , M_2 , M_7 , and M_8 for the first three stages, the maximum operating frequency can be increased. The self-oscillation frequencies of the second and the third stages are also increased due to a reduced delay time of the flip-flops. Since the output signal level of the first and the second stages are small and cannot be arbitrarily increased, the minimum operating frequency (which is the lowest frequency in the locking range) of the divide-by-128 circuit is also increased. The maximum speed of the divide-by-128 prescaler is predominantly determined by the first stage, while the minimum operating frequency is predominantly determined by the latter stages, whose input signal levels are smaller. Because the divider works in a frequency range over 77% of the maximum operating frequency, which is much larger than the VCO tuning range, the limitation imposed by the minimum frequency is not an issue.

B. Measurement Results

At 5.4 GHz, the prescaler, excluding the buffer formed by an inverter chain, consumes only 4.1 mW at $V_{DD} = 1.5$ V. The power consumption of the first stage is 1.65 mW, which is comparable to that of an analog frequency divider [11], while the latter stages consume only $\sim 1/5$ of the power of the prescaler in [11]. The maximum operating frequency can be increased by increasing V_{DD} and current [Fig. 6(a)]. As discussed above, when M_1 , M_2 , M_7 , and M_8 in the first three stages (divide-by-eight) are widened, the maximum operating frequency can be increased. By widening these transistors by $\sim 20\%$, a maximum operating frequency of 9.96 GHz is measured at 2.5-V V_{DD} and 7.36-mA total current for the first three stages. The output waveform to a $50\text{-}\Omega$ load for the second prescaler is shown in Fig. 6(b). Minimum peak-to-peak amplitude for the input signal versus operating frequency plots at different supply voltages (V_{DD}) for the second prescaler is shown in Fig. 7. The minimum peak-to-peak amplitude is ~ 40 mV at ~ 6.4 GHz when $V_{DD} = 2$ V. The performance of the prescalers is summarized in Table I.

Die photographs of the VCO using p^+ /n-well varactors and the divide-by-128 prescaler are shown in Fig. 8. The total area

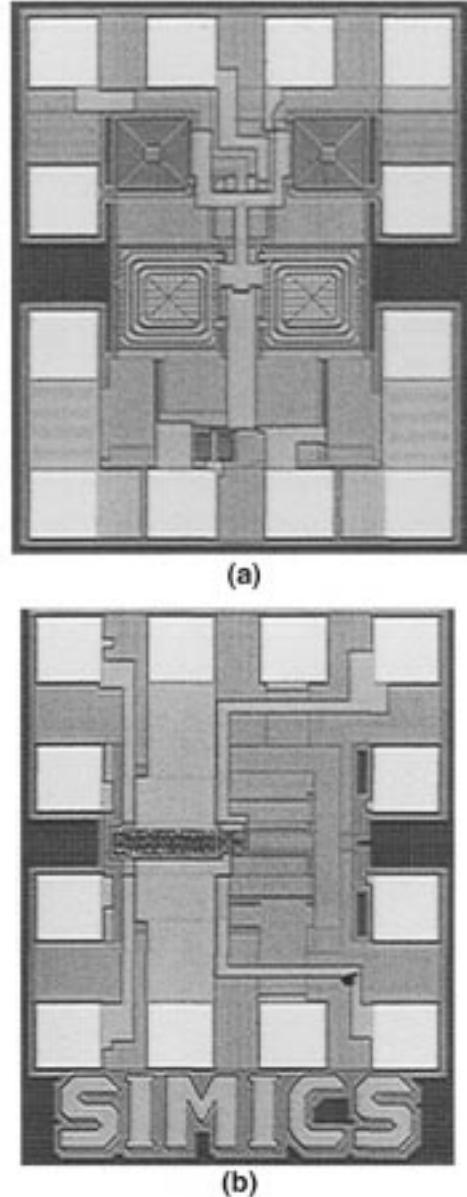


Fig. 8. (a) A die photo of the VCO using p^+ /n-well varactors. (b) A die photo of the divide-by-128 prescaler.

of the VCO including pads is $581 \times 470 \mu\text{m}^2$. The active area of the prescaler including internal bypass capacitors is $181 \times 244 \mu\text{m}^2$. To reduce the substrate coupling, all the bond pads have a polysilicon ground shield underneath, and empty areas are filled in with p -substrate contacts while not forming a closed loop around the inductors.

IV. CONCLUSION

Two 5.35-GHz integrated VCOs and two prescalers have been demonstrated. The pros and cons for using MOS and p^+ /n-well varactors for VCO applications were presented. The phase-noise flatness of the VCO using MOS varactors is less than 1 dB over the entire tuning range. At frequencies much higher than 5.35 GHz, an MOS varactor is preferred because of its higher Q . The low phase-noise performance and low power consumption of the VCOs and prescalers suggest that

integration of low-cost and low-power-consumption frequency synthesizers for high-bit-rate 5-GHz wireless applications is feasible in a digital 0.25- μ m CMOS process.

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